antares Advanced Test Technologies

Socket Signal Integrity – Impact from IC & Board

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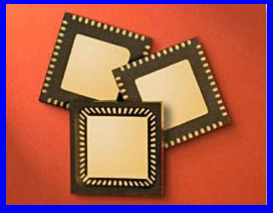
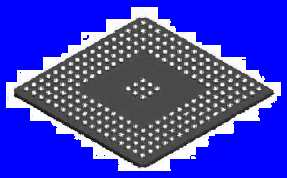
March 11-14, 2007
Hilton Phoenix East, Mesa Arizona

BiTS Burn-in & Test Socket Workshop

Outline

- ✓ Introduction
- ✓ QFN package + spring pin socket
- ✓ BGA package + spring pin socket
- ✓ LGA pad size vs. bandwidth
- ✓ Summary





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Introduction

- Package test system:

IC package + Contactor/socket + Load board

- Common practice to simulate SI performance separately
  - attempt to derive the system performance from individual sub-systems of loadboard, socket and package.
- In reality these components have EM coupling between each other. SI performance of each component is affected by other components.
- Analysis on system level coupling effects between components are presented.

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Spring pin socket for QFN package

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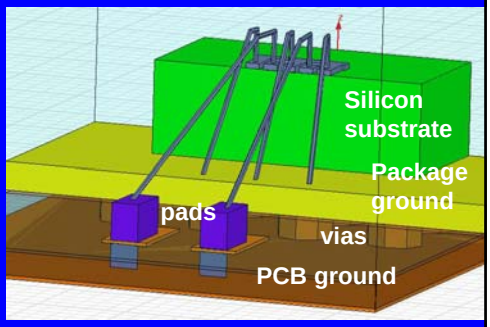
A Simple QFN Package Model

- Two signal paths formed by:
  - PCB pads
  - QFN pads
  - Bondwires
  - Signal pads on silicon
- Ground loop formed by:
  - PCB ground plane
  - 2x4 via array
  - QFN ground pad
  - Bondwires
  - Ground pads on silicon



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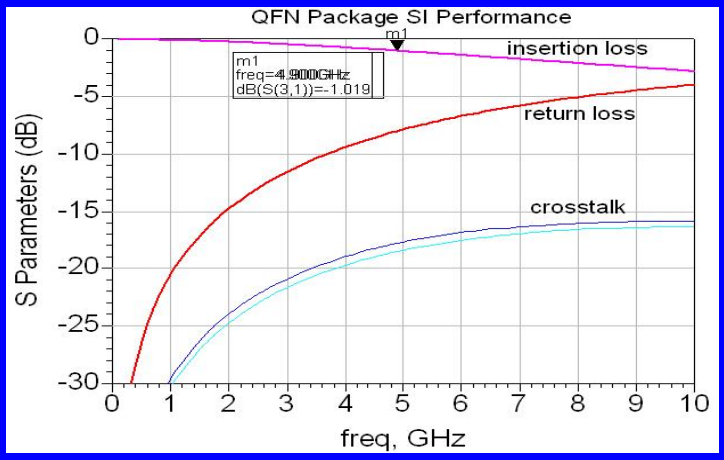
QFN Package Performance



Insertion loss (IL): IL = 1dB @4.9GHz
Return loss (RL): RL = 13dB@2.4GHz
Crosstalk (XT): XT = 30dB@1GHz

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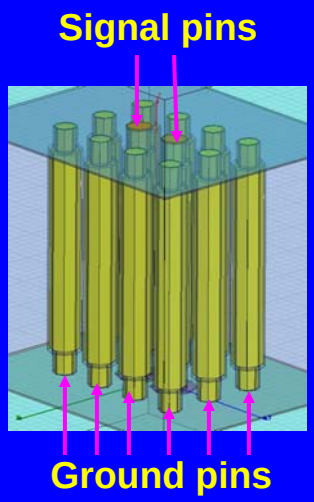
A High-speed Pin Array

- 3x4 pin array
- 2 signal pins + 10 ground pins
- Multi-conductor transmission line
- Bandwidth determined by characteristic impedance Z_0
  - Z_0 is function of pitch-to-diameter ratio and dielectric constant
- Pin array parameters:
  - length: 2.5mm
  - diameter: 0.3mm
  - pitch: 0.5mm



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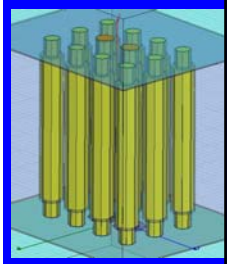
Pin Array Performance



- Max insertion loss 0~40GHz is 0.6dB
- 1dB bandwidth is greater than 40GHz

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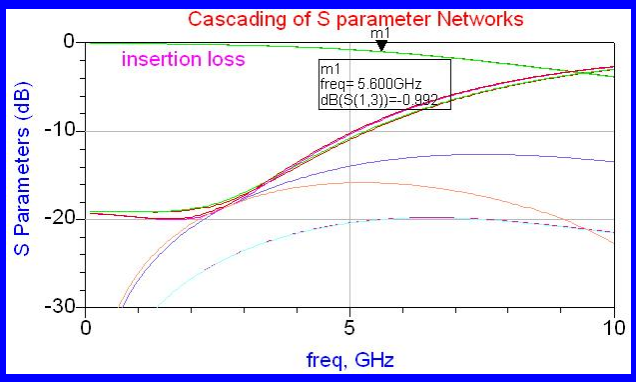
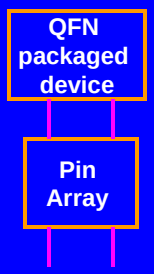
Cascaded Networks





- By cascading the QFN package and pin array networks, the overall system 1dB bandwidth is 5.6GHz
- It is higher than the bandwidth of QFN package
  - How could the bandwidth increase after inserting a pin array?

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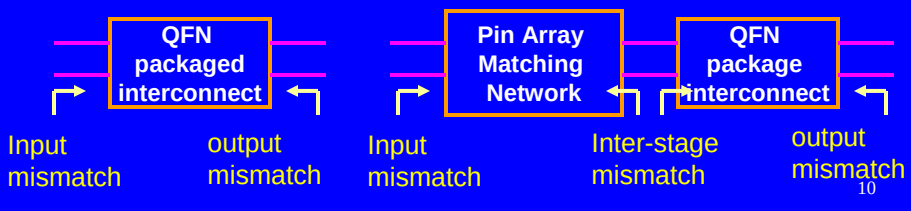
Matching Network

- pin array forms matching network
- two additional mismatch factors are introduced at input and output
  - In a near-lossless network, IL is mostly caused by reflection; as a result, reducing RL will yield better IL performance
  - Overall system bandwidth cannot in general be derived from arithmetic of sub-system bandwidth numbers



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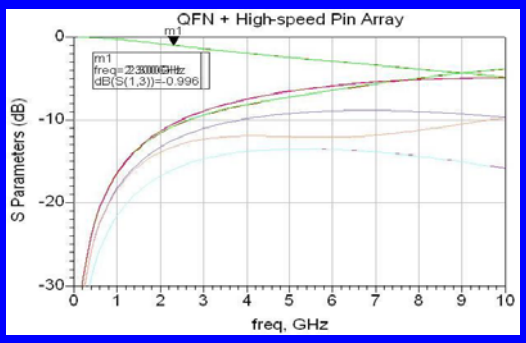
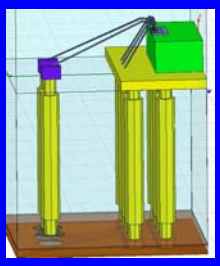
3D Full-wave EM Analysis





- 3D full-wave EM analysis (HFSS) of entire system
- 1dB bandwidth is 2.3GHz, less than half of QFN package bandwidth of 4.9GHz
- Bandwidth significantly lower than cascading network bandwidth of 5.6GHz.
- What has gone wrong?

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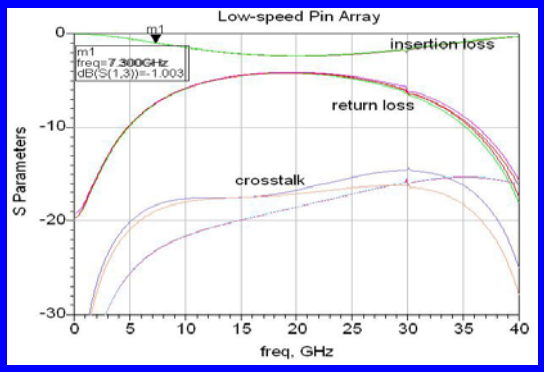
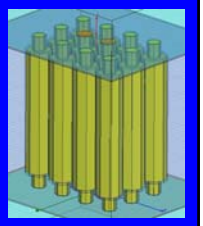
A Low-speed Pin Array





- 1dB bandwidth = 7.3GHz, significantly lower than the high speed pin array
  - Pin array parameters: length=2.5mm; diameter=0.4mm; pitch=0.5mm

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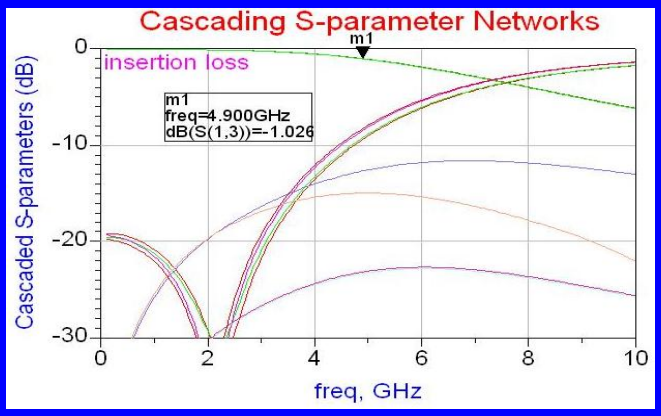
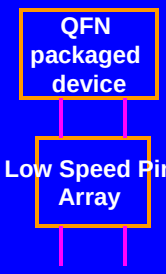
Cascading S Parameters





- By cascading QFN package and pin array sub-networks, overall system 1dB bandwidth is 4.9GHz
- It's the same as the bandwidth of the QFN package itself

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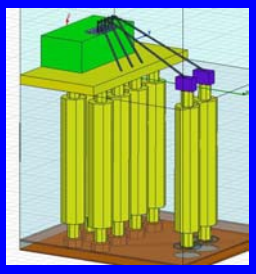
3D Fullwave EM Analysis



- 3D fullwave EM analysis of low-speed pin array plus the QFN package system
  - 1dB bandwidth = 2.5GHz
  - It is **higher** than the high-speed pin array bandwidth of 2.3GHz
  - It is about half of the cascading network bandwidth
- **How could a low-speed pin array has higher bandwidth than the high-speed pin array? (same QFN package)** 14

Observations

- QFN package itself has a 1dB bandwidth of 4.9GHz
- cascading S-parameter networks: the overall system bandwidth is equal to or higher than the bandwidth of the QFN package
- 3D fullwave EM analysis: the overall system bandwidth is significantly lower than the QFN package
- Low-speed pin has slightly better performance than the high-speed pin in the overall system (WHY?)
- 3D fullwave analysis reveals additional source of insertion loss from radiation
  - Pins surrounded by all ground pins has much less radiation

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Discussion – Cascaded Networks

- Cascaded network technique is often used in the calculation of overall system performance from individual sub-systems of PCB, socket and package
- In network analysis, the input/output ports are assumed to be terminated by infinitely long transmission lines

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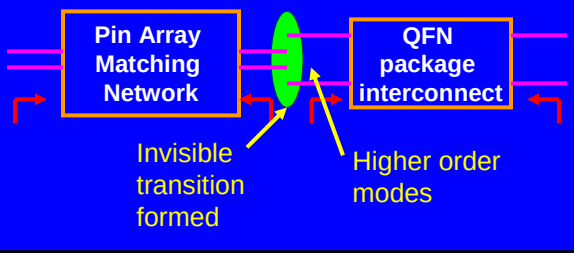
Cascaded Networks (cont.)

- when two networks of disparate interface geometries are cascaded, this important termination condition is violated
- An extra "invisible transitional network" has been created in the system, which characteristics are totally unaccounted for
  - Higher order modes exist in the vicinity of the transition



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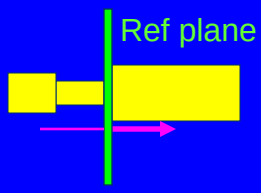
Discontinuity and Mismatch

- By separating a system at its discontinuity points, potentially large errors can be introduced due to impedance mismatch and higher order mode
- Discontinuities causes impedance mismatch; higher order modes EM fields exist in its vicinity
- when a reference plane is set up at these locations, the field patterns are greatly disturbed by the reference planes and port structure, resulting in potentially large errors



When system boundary is setup at discontinuity transitional locations, large errors can occur

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The Golden Rule

- When using "reference planes" to break a system into sub-systems, the planes must be located at **uniform transmission lines** with fair distance on both sides of the plane away from any discontinuity.
- The interface between socket and package is NOT in the middle of a uniform transmission line; in fact it is one of the most significant discontinuity points in the system

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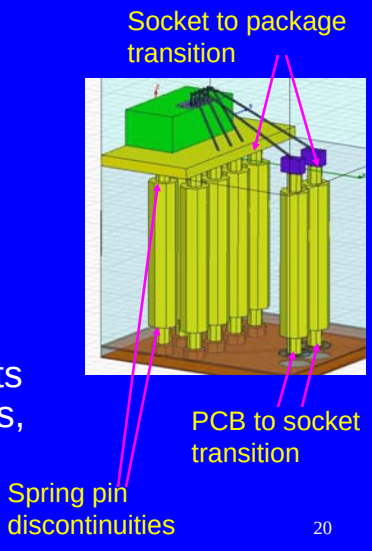
Socket Discontinuities

- Two biggest discontinuities in a socket system:
  - PCB to socket transition
  - Socket to package transition
- Spring pins also have discontinuities :
  - Change of diameter
  - From plunger to shell
  - From shell/plunger to pin tips
- By setting up input/output ports at these discontinuity locations, large errors usually occur



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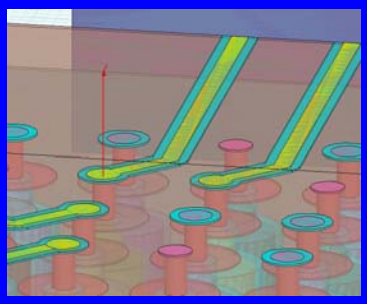
Port Setup

- To satisfy the fundamental requirements of port (reference plane) setup:
  - use microstrip or coplanar waveguide (CPW) transmission lines
  - setup the ports at fair distance away from any discontinuities of pad, via, dielectric boundary



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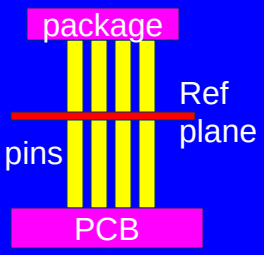
Port Setup – long pins

- For longer pins, reference planes can be setup at mid-section of pins
  - Satisfy uniform transmission line requirement
  - Electrical boundaries do not necessarily follow natural mechanical boundaries
  - Think out of the "box" and beyond the normal "boundaries"



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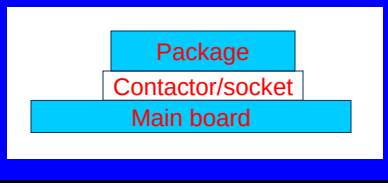
Board + Socket + Package

- In order to obtain accurate results on overall system bandwidth, it is highly desirable to **analyze the entire system** of load board + socket + package
- The input/output ports can be set up at locations of loadboard/package PCB traces, which are good uniform transmission lines
- This approach will guarantee the proper set up of the problem



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Spring pin socket for BGA package

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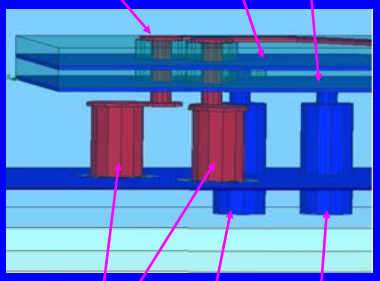
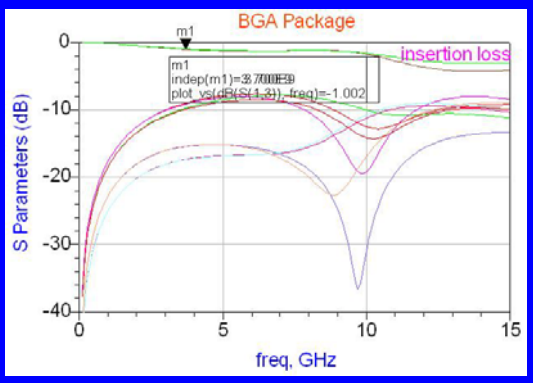
BGA Package Model





- 1dB bandwidth = 3.7GHz
- Usable frequency up to 10GHz

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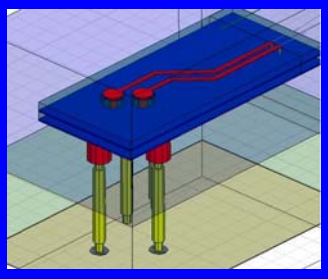
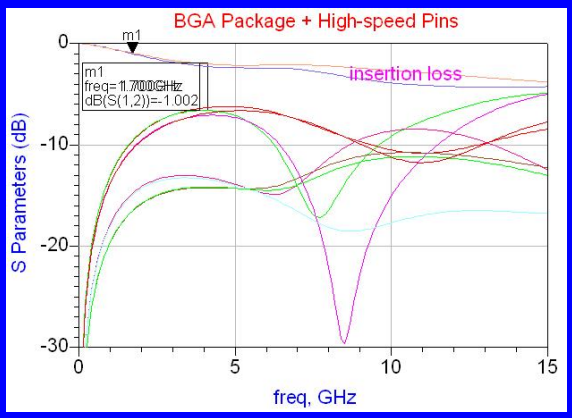
BGA Package + High-speed Pins





- **Using 40GHz high-speed pins with BGA package:**
  - **1dB bandwidth = 1.7GHz**
  - **Less than half of BGA package bandwidth**

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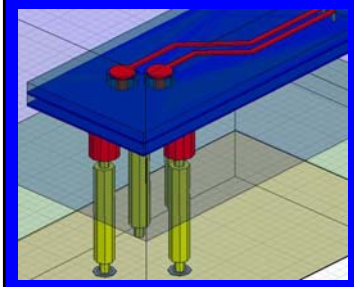
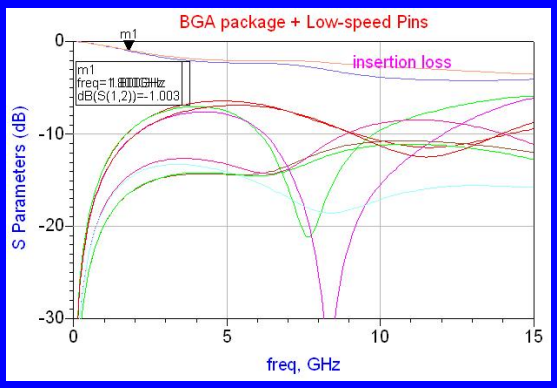
BGA Package + Low-speed Pins





- Using 7GHz low-speed pins with package:
  - 1dB bandwidth = 1.8GHz
  - Less than half of BGA package bandwidth
  - Higher than high-speed pin bandwidth

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Discussions

- Overall system performance of low-speed pins is better than high-speed pins
- BGA package bandwidth of 3.7GHz is reduced to 1.7GHz after inserting a 40GHz pin array; it is reduced to 1.8GHz after inserting a 7.3GHz pin array
- Why does the 7GHz low-speed pin array result in better performance than the 40GHz high-speed pin array?

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Discussions

- Bandwidth of "package+socket" system is not directly related to the individual sub-system bandwidth
- 3D EM effects must be simulated in one system
- Discontinuities between socket and package can only be accurately modeled in 3D full-wave analysis
- Radiation effects
- Changing pitch will completely change socket characteristic

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LGA Pad Size vs. Bandwidth

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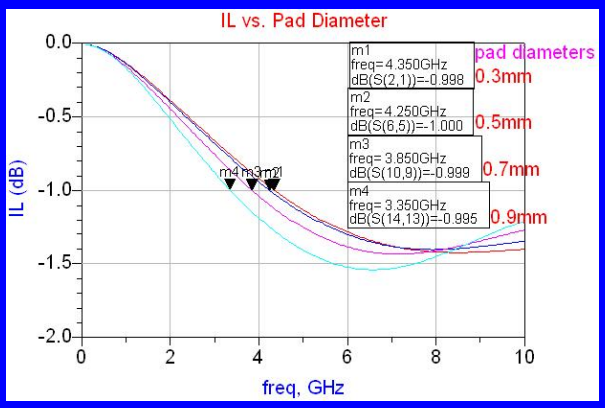
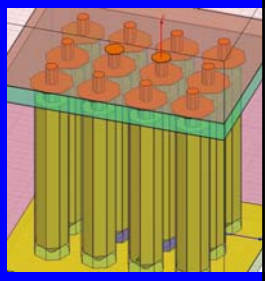
LGA Pad sizes vs. IL





- Pin array: 2 signals, 10 grounds
- Pad size sweep values: 0.3/0.5/0.7/0.9mm
- 1dB bandwidth: 4.35/4.25/3.85/3.35 GHz

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Discussion

- Very large pads are often used in LGA package for mechanical alignment tolerances
- These large pads have adverse effects on system bandwidth
- Large discontinuities and impedance mismatch exist at socket-to-package transition
- Degradation of IL cannot be easily overcome by spring pin design

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Summary

- The discontinuities at PCB-to-socket and socket-to-package transitions must be evaluated as an integrated part of the system
- Cascaded network approach may result in large errors if these discontinuities are not modeled properly
- Socket SI performance is NOT just determined by the socket itself; it is dependent on the package and PCB design
- To ensure best accuracy, model the PCB+socket+package as an integrated system using 3D full-wave EM tools

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