
antares
Advanced Test Technologies
Minimizing Socket & Board Inductance using a Novel decoupling Interposer
2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007
BiTS
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James Zhou, Hongjun Yao


• It is better to uncover a little than to cover a lot.
• Eric Bogatin , SI Artisan
» www.bethesignal.com
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Performance Limiting Noise

- Power ground voltage droop (Rail Collapse)
- Simultaneous Switching Noise (SSN – Ground Bounce)

- PDS Components
- Board – Socket – DUT package – decoupling components

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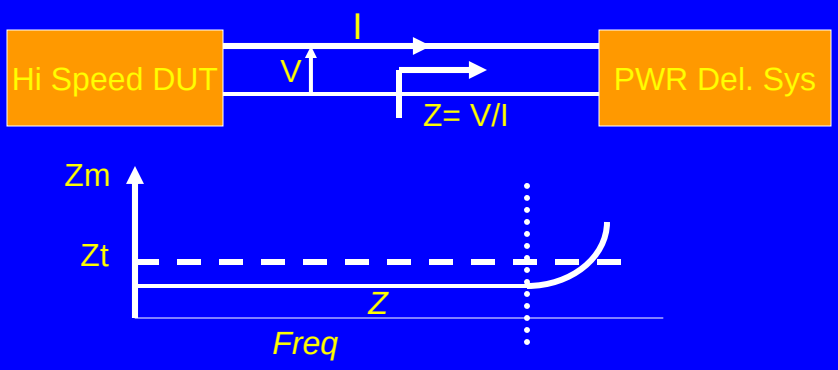

PDS has to distribute the power to the chip
Has to keep the ripple (noise) to spec ~ 5%
Can not droop all the way to the BW of DUT

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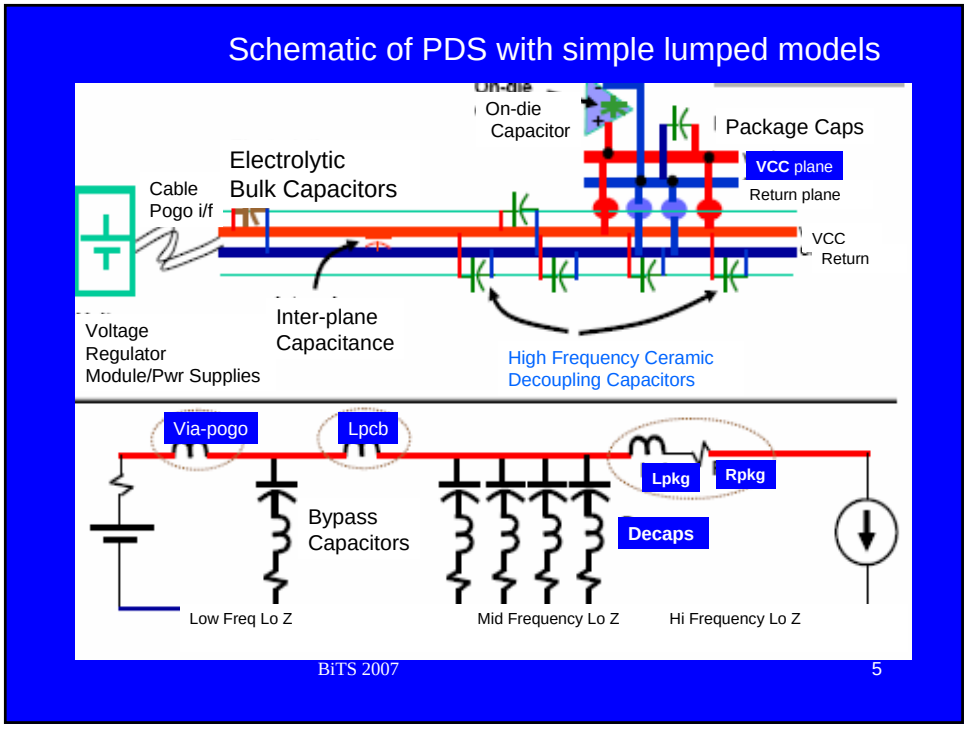
Schematic of PDS with simple lumped models
On-die Capacitor
Package Caps
Electrolytic Bulk Capacitors
VCC plane
Return plane
Cable Pogo i/f
VCC Return
Voltage Regulator Module/Pwr Supplies
Inter-plane Capacitance
High Frequency Ceramic Decoupling Capacitors
Via-pogo
Lpcb
Lpkg
Rpkg
Bypass Capacitors
Decaps
Low Freq Lo Z
Mid Frequency Lo Z
Hi Frequency Lo Z
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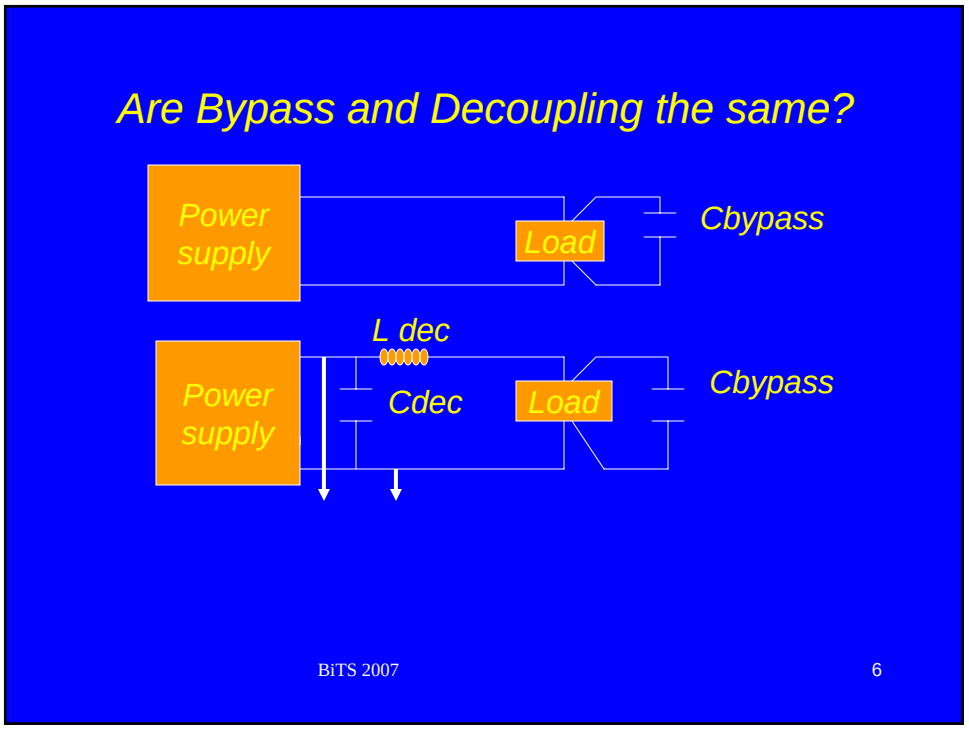
Are Bypass and Decoupling the same?
Power supply
Load
Cbypass
L dec
Power supply
Cdec
Load
Cbypass
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Basic PDS Design Strategy

Determine required PDS impedance

$Z = \Delta V / \Delta I$

Determine the frequency for the PDS alone

$Fpds = Z / 2\pi L\ pds$

Bypass $C = 1 / 2\pi FpdsZ$

Determine how much L we can handle at Fmax

$L = Z\ Tr/\pi$

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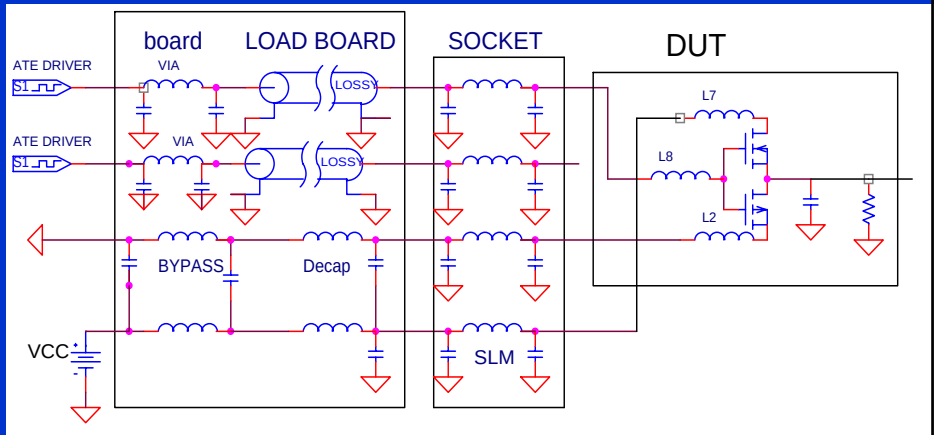
Reviewing SSO/SSN/Ground Bounce



Test Cell Schematic

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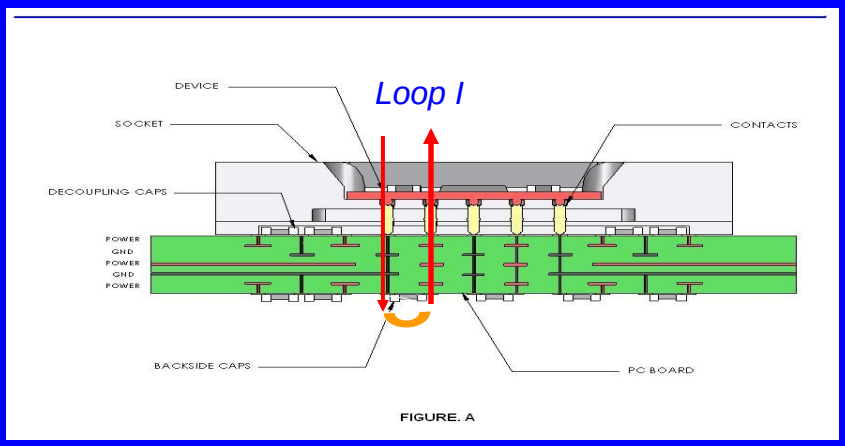

FIGURE. A

$\frac{Vgb}{Vs} = n \times \frac{Lnet}{Tr \times Zo}$

3 nets, 5nH, 0.5ns Tr, 50 ohms
60% Vgb!

Inductance is like Kryptonite!

- For Digital Designers of high speed test cells,
- Inductance is the bane of good designs

Capacitance is like Free Beer!

Simulation of the impact of Bypassing

- 8 layer FR4 board; 0.635mm dielectric
- 5 .01uF caps on bottom of the board
- 1 power via; .25mm dia.; 0.5mm antipad
- Chip mounted directly to the board
- Chip in a socket mounted to the board
- Chip in a socket with the .01uF caps

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Load Configuration

- 10 ohm resitive load to draw 100ma
  - from 1v supply
- 0.1nF on chip bypass on each power pin
- Load is turned on at 5ns,
  - the Tr is 200ps

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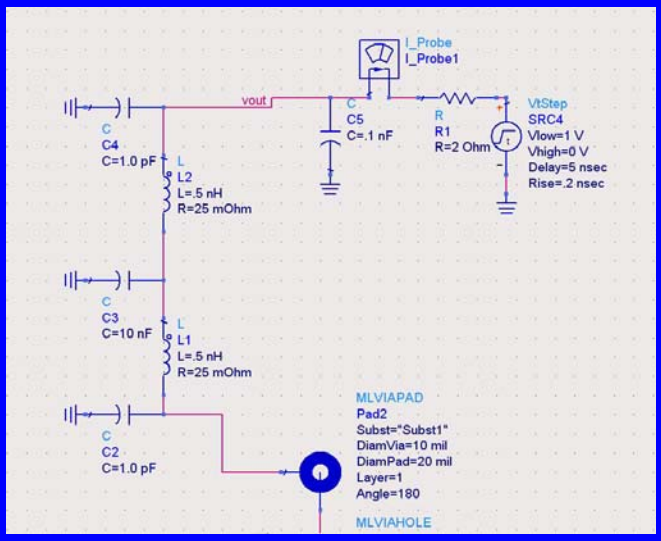
Spring Pin and Load Model

- *Spring Pin is modeled as a CLC pi network*
- *There is a 10nF bypass in the interposer*



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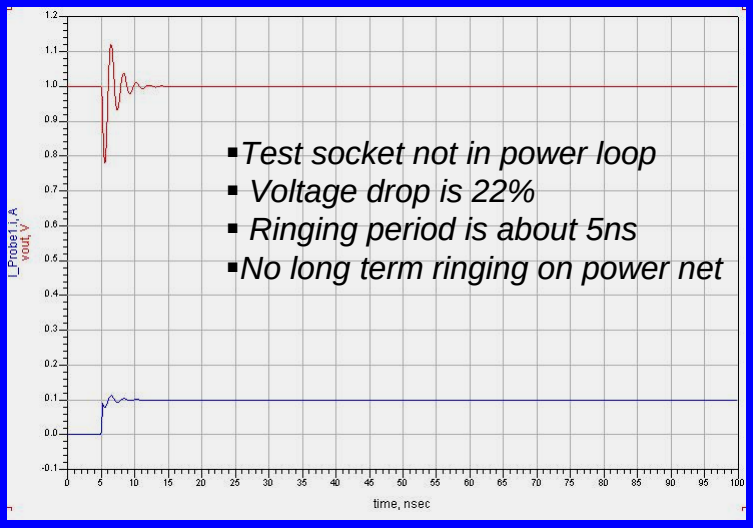
Case 1. Chip mounted to the PCB



- *Test socket not in power loop*
- *Voltage drop is 22%*
- *Ringing period is about 5ns*
- *No long term ringing on power net*

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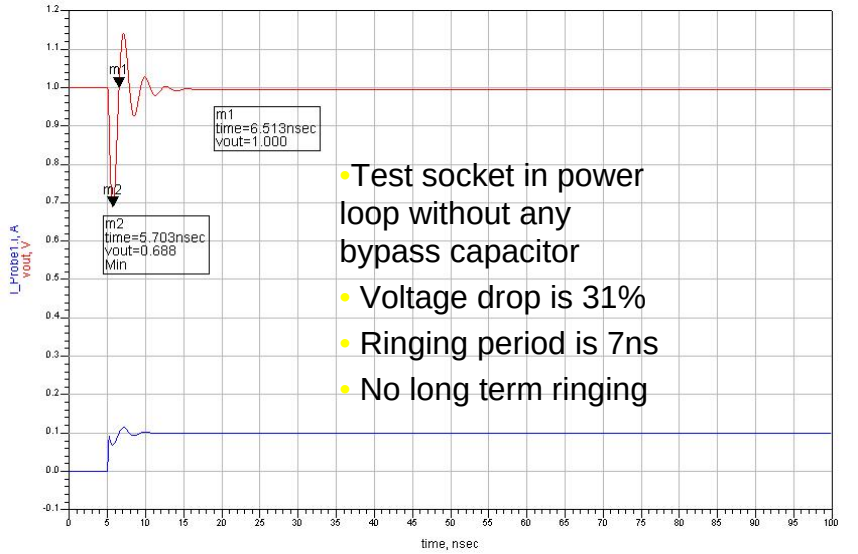
Case II: Using Socket with no bypass



- Test socket in power loop without any bypass capacitor
- Voltage drop is 31%
- Ringing period is 7ns
- No long term ringing

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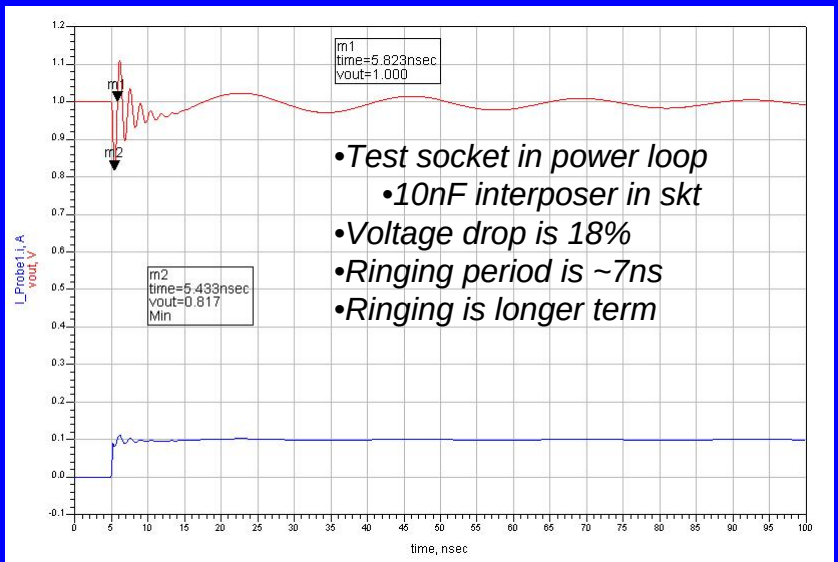
Case III: Contactor with bypass interposer



- *Test socket in power loop*
  - *10nF interposer in skt*
- *Voltage drop is 18%*
- *Ringing period is ~7ns*
- *Ringing is longer term*

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Observations

- 1nH test contactor increases the power drop from 22% to 31%
- 10nF bypass cap reduces the power drop to 18%
- The built-in bypass cap and the spring pin inductance causes some long term ringing on the power net..

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Interposer Position

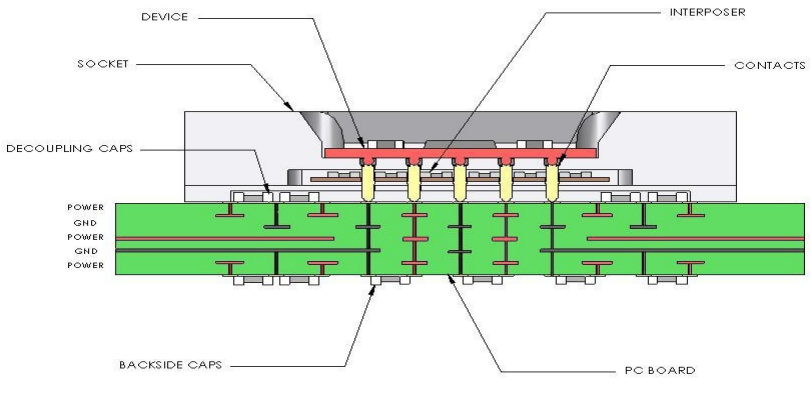

FIGURE. B

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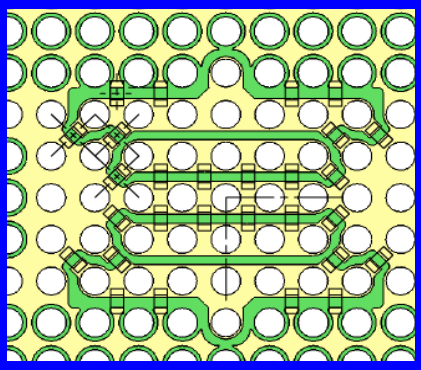
Decoupling Interposer



Drawing of Interposer

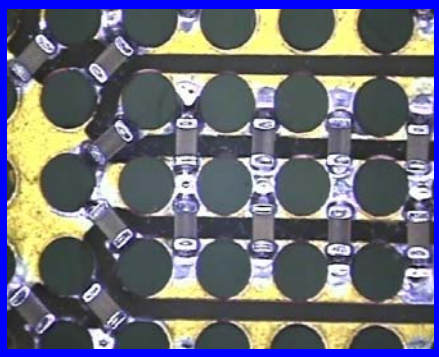


Photo of Interposer – 1mm pitch

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Socket **without** Built-in Decap

WELLS LOW INDUCTANCE SOCKET
Data=Address tCYC=4.0ns Vref=.75 VCCQ=1.50V "K/K# CLOCK SKEW TEST"
K/K# Skew vs VCCCY7C1414V18 QDR2-2bx36 36M=512Kx2x36

```
                -.75    -.5     -.25     0      0.25     0.5     0.75ns
          VCC(V)  +--------+--------+--------+--------+--------+--------+-
2.100V    |.............PPPPPPPPPPPPPP.PP.PPPPPPPPP.P.P.P.P.PPPPP.PPPP|
2.075V    |.............PPPPPPPPPP.PPPPPPPPPP.PPPPP.P.P..PPPP.PPPP.PP.|
2.050V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP.PPP..P.PPPPPPPPPP..PP|
2.025V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP..P.PPP.P.PPPPPPPPPP
2.000V    |.............PPPPPPPPPPPP.PPPPPPPP.PPPPPP.PPPP..P..PPPPP.P.|
1.975V    |.............PPPPPPPPPPPP.PPPPPPPPPPPPPP..PPP.P.P.PPPPPP.PP|
1.950V    |.............PPPPPPPPPPPPPPPPPP.PPPPPPPPP.P.P.P.P..PPP.PPP.|
1.925V    |.............PPPPPPPPPPPPPPPPP.PPPP.PP.PPP..PP.PP.PPPPP.P.P|
1.900V    |.............PPPPPPPPPPPPPPPPPPPPPPPPPP.PPP.PPP.PP..PPPPPP|
1.875V    |.............PPPPPPPPPP.PPPPP.PPPPP.PPPPP.P.PPP.P.PPPPPP.PP|
1.850V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP.PPP.PPP.P.P..PPPPPPP|
1.825V    |.............PPPPPPPPPPPPPPPP.P.P.PPP.PP..P.PPPP.PP.PPPPPPP|
1.800V    |.............PPPPPPPPPPPPPPPPPPPPPPP.P.PPP..PPP.P..PP.PPPP.|
1.775V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP.P.PPPPPP.PPPP.PPPPPP|
1.750V    |.............PPPPPPPPPPPPPPP.PPPPPPPPP.P.PPP.PPP.P..PPP.P.|
1.725V    |.............PPPPPPPPPPPP.PP.PPPPPP.P.PP.PP.P.P.PP.P..P.P.|
1.700V    |.............PPPPPPPPPPPPPPPPPPP.PPPPPP.PP.PP.P.PP.PPPP.PP|
1.675V    |.............PPPPPPPPPP.PPPPPPPPPPPP.PP.PP.PPPP.PPPP.PPPPPP|
1.650V    |.............PPPPPPPPPPPPPPPPPPPPPPPPPP.P.PP.PPP.PPPPPPPPP|
1.625V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP.PP.PP.P.PP.PPPPPPP.|
                +--------+--------+--------+--------+--------+--------+-
                -.75    -.5     -.25     0      0.25     0.5     0.75ns
                                  K/K# Skew (ns)
```

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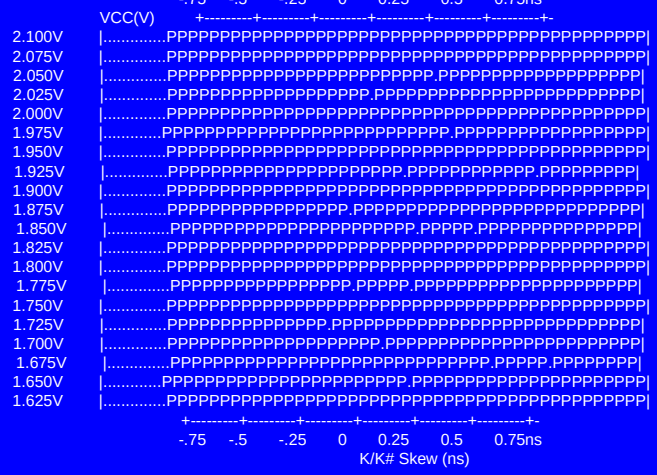
Paper #2

Socket with Built in Decoupling

SOCKET WITH BUILT IN DECOUPLING
Data=Address tCYC=4.0ns Vref=.75 VCCQ=1.50V "K/K# CLOCK SKEW TEST"
K/K# Skew vs VCCCY7C1414V18 QDR2-2bx36 36M=512Kx2x36



Summary

- Inductance is the number one cause of noise and the primary cause of rail collapse
- A well designed cap network will counteract the Inductance
- The closer the caps to the noise source; the more effective they are

- **Thanks to Cary Stubbles of Cypress for his support.**